REMARKS

I. Status of the Application

Claims 15 and 17-34 are pending in this application. In the January 9, 2006 office action, the Examiner:

A. Objected to the claims because of informalities;

B. Rejected claims 15 and 17-34 under 35 U.S.C. § 103(a) as allegedly being obvious over U.S. Patent Publication No. US 2003/0006892A1 by Alessandria et al. (hereinafter "Alessandria") in view of Kimura (U.S. Pat. 6,851,849), Hartwick (U.S. Pat. 4,881,024), Kumar (U.S. Pat. 6,855,981), Zeiler (U.S. Pat. 4,937,470) and/or Pavlin (U.S. Pat. 5,438,286).

In this response, applicants have amended claims 18 and 19 and have canceled claim 17, without prejudice, to address the informalities noted by the Examiner. Applicants have also added new claim 35. Applicants respectfully traverse the prior art rejections and request reconsideration of the application in view of the following remarks.

II. The Objections to the Claims are Moot

The Examiner objected to the claims for informalities relating to claims 17 and 19. The informalities in these claims inadvertently arose as a result of the amendments to the claims made in the Response to Office Action dated October 31, 2005. In this Response, claim 17 has been canceled, and claim 19 has been amended to depend from claim 15. Claim 18 has also been amended to depend from claim 19 and to replace the words "constant voltage element" with "Zener diode". It is respectfully submitted that the amendments adequately

address the objections of the Examiner in the January 9, 2006 office action.

Thus, it is believed that the objection to claims 17 and 19 are now moot.

III. Obviousness Rejection of Claim 15

Claim 15 stands rejected as allegedly being rendered obvious over Alessandria in view of Pavlin. As will be discussed below in detail, there is no legally sufficient motivation or suggestion to combine Alessandria and Pavlin as proposed by the Examiner. Alternatively, the proposed combination does not arrive at the claimed invention. As a consequence, it is respectfully submitted that the obviousness rejection of claim 15 should be withdrawn.

A. Present Invention

The discussion of claim 15 from the prior Response to Office Action is reproduced here for the Examiner's convenience.

Claim 15, as amended, is directed to a MOSFET circuit comprising a first MOS transistor, a second MOS transistor and a Zener diode. The number of cells in the second MOS is less than the number of cells in the first MOS, and the source-drain paths of each transistor are connected in parallel between a voltage source and a reference potential. The Zener diode is coupled between a gate of the first MOS transistor and a gate of the second MOS transistor.

B. Alessandria

Alessandria is directed to a power device having an integrated voltage stabilizing circuit comprising a MOS transistor that is connected in parallel to a circuit that is integrated

in a power device. (Alessandria at Abstract). To this end, one embodiment employs a MOS transistor 22 having a drain coupled to a control circuit 23 and to an input voltage. The MOS transistor 22 also has a gate coupled to the input voltage via a Zener diode 20. (See *id.* at Fig. 5). In another embodiment, the above circuit is modified to include a current mirror coupled between the input voltage and the drain of the MOS transistor 22. (See *id.* at Fig. 10).

C. Pavlin

Pavlin is directed to a circuit for the detection of an open load for a power MOS transistor designed to operate in a switching mode. Pavlin is not directed to voltage stabilization. (Pavlin at Abstract and cols. 1 & 2).

D. The Proposed Combination

In the January 9, 2006 office action, the Examiner appears to have admitted that Alessandria does not teach the use of a second transistor having less cells than the first transistor, although the Examiner alleges that Alessandria otherwise teaches the limitations of claim 15. (January 9, 2006 office action at p.2). The Examiner addresses the shortcoming of Alessandria with respect to the relative number of cells in the MOS transistors by citing teachings of Pavlin.

As an initial matter, it appears that the Examiner's application of Alessandria contains inadvertent errors, possibly typographical. In particular, the Examiner alleged that "figure 10 of Alessandria shows a MOSFET circuit comprising: a first transistor (23); a second MOS transistor (22) connected in parallel, a Zener diode (20) coupled between the gates of the first and second MOS transistors." (*Id.*) Applicants disagree. Fig. 10 shows a MOS transistor

(22) and a current mirror, but *no* element, much less a transistor, labeled with the reference numeral "23". It would appear that the Examiner has made an inadvertent error and was intending a different explanation.

There appear to be three possible intended meanings of the Examiner: 1) The Examiner assumed that the circuit of Fig. 10 should be connected to a block 23 similar to the circuit of Fig. 5; 2) the Examiner actually intended to reference Fig. 5 of Alessandria, and not Fig. 10; or 3) The Examiner meant to state that the first transistor was one of the current mirror transistors of Fig. 10.

1. Assuming a Block 23 is Added to Fig. 10

If it is assumed that the output of the circuit of Fig. 10 is connected to a block labeled 23 as is the case with the circuit Fig. 5, and if it is assumed that this is the basis of the Examiner's rejection of claim 15, then proposed combination of Alessandria and Pavlin does not arrive at the claimed invention.

In particular, the claimed combination does not include first and second transistors coupled in parallel and having a Zener diode coupled between their two gates. To this end, the Examiner has alleged that element 23 is the first transistor. However, Alessandria clearly teaches that the "reference numeral 23 designates the control circuit integrated in a power device" (Alessandria at paragraph [0065]). The "control circuit 23" of Alessandria does not constitute or include a parallel connected transistor, and certainly does not constitute or include a parallel connected MOS transistor having a gate connected to the Zener diode 20.

Alessandria does not therefore teach a first and second transistor having drain-source connections connected in parallel, wherein the Zener diode is connected between their

respective gates. Thus, even if Alessandria were modified as proposed by the Examiner to incorporate the different numbers of cells taught by Pavlin, the resulting combination would not include first and second transistors (and Zener diode) coupled as claimed. For this reason, it is respectfully submitted that the rejection of claim 15 over Alessandria and Pavlin is in error and should be withdrawn.

2. Assuming the Rejection is Over Fig. 5 of Alessandria

If the Examiner intended to cite Fig. 5, and not Fig. 10 of Alessandria, then it is respectfully submitted that the rejection should be withdrawn for reasons similar to those discussed above. Namely, Fig. 5 of Alessandria does not show first and second MOS transistors and Zener diode, coupled as claimed. The control circuit 23 of Fig. 5 does not constitute a parallel-connected MOS transistor. Thus, the proposed combination does not arrive at the invention of claim 15.

3. Assuming the First MOS Transistor is Part of the Current Mirror

If the Examiner intended to allege that one of the current mirror transistors of Fig. 10 of Alessandria constitutes the claimed first MOS transistor, then there is no motivation or suggestion to modify Alessandria as proposed.

It is initially noted that the circuits of Alessandria and Pavlin serve vastly different purposes, and the prior art does not fairly suggest that the advantages taught by Pavlin of using different numbers of cells in separate transistors would serve any purpose in the circuit of Alessandria.

In particular, Pavlin teaches an *open load detection* circuit that has a very low detection threshold. The low detection threshold is desirable "in order to differentiate the case when the charging current is low because the load has a high value from the case when the current is low, or zero because the load is open" (Pavlin at col. 1, lines 52-58). To achieve a low detection threshold, Pavlin introduces a composite transistor TP made up of two MOS transistors TP1 and TP2 having separately driven gates, and vastly different numbers of cells. (*Id.* at col. 4, lines 23-62).

Alessandria is not an open load detection circuit. Alessandria does not have a need for a low detection threshold similar to Pavlin. Fig. 10 of Alessandria is silent with respect to low current detection thresholds, and none of the prior art teaches that a voltage stabilization circuit such as that of Alessandria has or requires a low detection threshold. The teachings of Pavlin simply have no application to Alessandria.

For this reason, it is respectfully submitted that there is no legally sufficient motivation or suggestion to combine Alessandria as proposed. The rejection is therefore in error and should be withdrawn.

IV. Claim 19

Claim 19 stands rejected as being obvious over Alessandria in view of Pavlin in further view of Zeiler. Claim 19 depends from and incorporates all of the limitations of claim 15. As an initial matter, the proposed modification of Alessandria and Pavlin with Zeiler does not address the deficiencies of the Alessandria and Pavlin discussed above in connection with claim 15. Accordingly, it is respectfully submitted that the rejections of claim 19 should be withdrawn for at least the same reasons as those set forth above in connection with claim 15.

In addition, claim 19 is patentable for additional reasons. Claim 19 includes a limitation of a resistor connected parallel to the Zener diode that is disposed between the gates of the two claimed transistors. The Examiner admitted that Alessandria and Pavlin did not teach such a parallel resistor, but instead relied on a further combination of Zeiler to provide such teaching. (January 9, 2006 office action at pp.2-3) In particular, the Examiner proposed modifying Alessandria and Pavlin with Zeiler using the following reasoning:

> The circuit of . . . Alessandria has a limitation that the voltage applied to the gate of transistor (22) only happens when the input voltage (Vin) is high enough to reverse biased Zener (20). Figure 1 of Zeiler shows a Zener diode (44) having a resistor (46) coupled in parallel with it for continuously controlling the first MOS transistor (48) and for limiting the voltage applied to the gate of the first MOS transistor. Therefore, it would have been obvious for one of ordinary skill in the art to replace the single diode (20) of Alessandria with the diode and the resistor taught by Zeiler for continuously controlling the first MOS transistor (48) and for limiting the voltage applied to the gate of the transistor.

(January 9, 2006 office action at p.3)

Applicants respectfully disagree that the prior art fairly suggests that Alessandria has a "limitation" because the voltage applied to the gate of transistor (22) only happens when the input voltage (Vin) is high enough to reverse biased Zener (20). There is no teaching in the prior art that the voltage stabilization circuit of Alessandria suffers any detriminent from this characteristic, as alleged by the Examiner. Although the parallel-connected resistor provides advantages in Zeiler, the Zener diode of Zeiler is not part of a voltage stabilization circuit similar to Alessandria. Instead, the Zener diode of Zeiler is part of a *gate driver* circuit of a switching power transistor. (Zeiler at Fig. 1).

There is no teaching in the art that a *voltage stabilization circuit*, such as that taught by Alessandria, is "limited" or operates sub-optimally because it requires a Zener diode drop before turning on the gate of a MOSFET. The purposes of the MOSFET in Alessandria and the purposes of the MOSFET in Zeiler are so vastly different that one of ordinary skill in the

art would not be motivated to modify the Alessandria circuit to include a resistor parallel to the Zener diode such as is taught by Zeiler.

Thus, in addition to the reasons set forth above in connection with claim 15, it is respectfully submitted that claim 19 is allowable over the prior art because there is no motivation or suggestion to combine Zeiler with Alessandria and Pavlin.

V. Claims 18 and 20-23

Claims 18 and 20-23 stand rejected as allegedly being obvious over at least the combination of Alessandria, Pavlin and Zeiler discussed above in connection with claim 19. Claims 18 and 20-23 all depend from claim 19 and therefore incorporate the same limitations. Accordingly, it is respectfully submitted that the prior art rejections of claims 18 and 20-23 should be withdrawn for at least the same reasons as those set forth above in connection with claims 15 and 19.

VI. Claims 24 and 30

The Examiner rejected claims 24 and 30 over Alessandria and Pavlin using substantially the same reasoning as that applied to the rejection of claim 15. (January 9, 2006 office action at pp.4-5) As discussed above, the rejection of claim 15 over Alessandria and Pavlin is in error. Accordingly, for at least the same reasons as those set forth above in connection with claim 15, it is respectfully submitted that the rejection of claims 24 and 30 over Alessandria and Pavlin are in error and should be withdrawn.

VI. Claims 25-29 and 31-34

Claims 25-29 and 31-34 were rejected as being obvious over Alessandria in view of Pavlin and, in some cases, other references. Claims 25-29 and 31-34 all depend from and incorporate all of the limitations of their base claims 24 or 30. As discussed above, claims 24 and 30 are patentable over the prior art for at least the same reasons as those set forth above in connection with claim 15. Accordingly, it is respectfully submitted that the rejections of claims 25-29 and 31-34 should be withdrawn for at least the same reasons as those set forth above in connection with claims 15, 24 and 30.

VII. New Claim 35

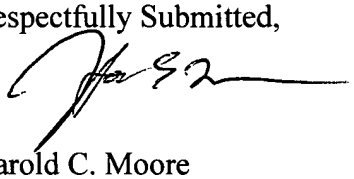
New claim 35 has been added, and includes a limitation identifying a relationship between a control input to the circuit and the Zener diode. This limitation recites that the Zener diode is forward biased from the control input to the second MOS transistor. This relationship is plainly shown in Fig. 1 of the Application as filed.

Claim 35 depends from claim 15 and is allowable for at least the same reasons. Moreover, Alessandria does not disclose a Zener diode forward biased from a control input of the circuit to the second MOS transistor. Accordingly, for reasons independent of claim 15, claim 35 is allowable over the prior art.

VIII. Conclusion

For all of the foregoing reasons, it is respectfully submitted that the application is in a condition for allowance. Favorable reconsideration and allowance of this application is, therefore, earnestly solicited.

Respectfully Submitted,



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